REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

Prepared in accordance with ASME Y14.24

Vendor item drawing

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PMIC N/A	**PREPARED BY** Phu H. Nguyen	**DLA LAND AND MARITIME** **COLUMBUS, OHIO 43218-3990** **http://www.landandmaritime.dla.mil/**
Original date of drawing YY MM DD 13-01-22	**CHECKED BY** Phu H. Nguyen	**TITLE** MICROCIRCUIT, DIGITAL, 4Ω R_{ON}, 4-CHANNEL ±15 V/+12 V/±5 V *i*CMOS MULTIPLEXERS, MONOLITHIC SILICON
	APPROVED BY Thomas M. Hess	
	SIZE **A** **CODE IDENT. NO.** **16236**	**DWG NO.** **V62/12652**
	REV	**PAGE** 1 **OF** 18

AMSC N/A

5962-V043-13

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance 4 Ω RON, 4-/8-channel ±15 V/+12 V/±5 V *i*CMOS multiplexers microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/12652	-	01	X	B
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	ADG1409-EP	4 Ω RON, 4-channel ±15 V/+12 V/±5 V *i*CMOS multiplexers

1.2.2 Case outline(s). The case outlines are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	16	JEDEC MO-153-AB	Think Shrink Small Outline Package

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

1.3 Absolute maximum ratings. 1/

V_{DD} to V_{SS} ..... 35 V
V_{DD} to GND ..... -0.3 V to +25 V
V_{SS} to GND ..... +0.3 V to -25 V
Analog inputs, Digital inputs ..... V_{SS} -0.3 V to V_{DD} + 0.3 V or 30 mA, whichever occurs first 2/
Peak current, S or D ..... 350 mA (Pulsed at 1 ms, 10% duty cycle maximum)
Operating temperature range: ..... -55°C to +125°C
Storage temperature range ..... -65°C to 150°C
Junction temperature ..... 150°C
θ_{JA} ..... 150.4 °C/W
θ_{JC} ..... 50 °C/W
Lead temperature soldering:
Vapor phase (60 sec)..... 215°C
Infrared (15 sec)..... 220°C
Continuous current per channel, S or D ..... See table below + 10%

Test	Test conditions	Limits			Unit
		25°C	55°C	125°C	
Continuous current, S or D 3/					
15 V dual supply	V_{DD} = +13.5 V, V_{SS} = -13.5 V	140	85	45	mA max
12 V dual supply	V_{DD} = 10.8 V, V_{SS} = 0 V	120	75	40	
5 V dual supply	V_{DD} = +4.5 V, V_{SS} = -4.5 V	115	70	40	

2. APPLICABLE DOCUMENTS

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JEP95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at http:/www.jedec.org or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201.)

1/ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
2/ Over voltages at A, EN, S, or D will be clamped by internal diodes. Current should be limited to the maximum ratings given.
3/ Guaranteed by design, not subject to production test..

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Terminal function. The terminal function shall be as shown in figure 3.

3.5.4 Truth table. The truth table shall be as shown in figure 4.

3.5.5 Functional block diagram. The functional block diagram shall be as shown in figure 5.

3.5.6 On resistance. The On resistance shall be as shown in figure 6.

3.5.7 Off leakage. The Off leakage shall be as shown in figure 7.

3.5.8 On leakage. The On leakage shall be as shown in figure 8.

3.5.9 Address to output switching times, $t_{TRANSITION}$. The address to output switching times, $t_{TRANSITION}$ shall be as shown in figure 9.

3.5.10 Break before make time delay, t_{BBM}. The break before make time delay, t_{BBM} shall be as shown in figure 10.

3.5.11 Enable delay, t_{ON} (EN), t_{OFF} (EN). The Enable delay, t_{ON} (EN), t_{OFF} (EN) shall be as shown in figure 11.

3.5.12 Charge Injection. The charge Injection shall be as shown in figure 12.

3.5.13 Off isolation. The Off isolation shall be as shown in figure 13.

3.5.14 Channel to Channel crosstalk. The Channel to Channel crosstalk shall be as shown in figure 14.

3.5.15 Insertion loss. The Insertion loss shall be as shown in figure 15.

3.5.16 THD + Noise. The THD + Noise shall be as shown in figure 16.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Test conditions **15 V Dual Supply** 2/	Limits						Unit
			+25°C			-55°C to +125°C			
			Min	Typ	Max	Min	Typ	Max	
Analog switch									
Analog signal range						V_{SS}		V_{DD}	V
On Resistance	R_{ON}	V_S = ±10 V, I_S = -10 mA, See FIGURE 6		4					Ω
		V_{DD} = +13.5 V, V_{SS} = -13.5 V			4.7			6.7	
On resistance match between channels	Δ R_{ON}	V_S = ±10 V, I_S = -10 mA		0.2					Ω
					0.78			1.1	
On resistance Flatness	$R_{FLAT(ON)}$	V_S = ±10 V, I_S = -10 mA		0.5					Ω
					0.72			0.92	
Leakage currents (V_{DD} = +16.5 V, V_{SS} = -16.5 V)									
Source off leakage	I_S (Off)	V_S = ±10 V, V_D = ∓10 V; See FIGURE 7		±0.04					nA
					±0.2			±5	
Drain off leakage	I_D (Off)	V_S = ±10 V, V_D = ∓10 V; See FIGURE 7		±0.04					
					±0.45			±30	
Channel On leakage	I_D, I_S (On)	V_S = V_D = ±10 V, See FIGURE 8		±0.1					
					±1.5			±30	
Digital inputs									
Input high voltage	V_{IH}					2.0			V
Input low voltage	V_{IL}							0.8	
Input current	I_{NL} or I_{NH}	V_{IN} = V_{GND} or V_{DD}		±0.005					µA
								±0.1	
Digital input capacitance	C_{IN}			4					pF

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test conditions **15 V Dual Supply - Continued** 2/	Limits						Unit
			+25°C			-55°C to +125°C			
			Min	Typ	Max	Min	Typ	Max	
Dynamic characteristics 3/									
Transition time	$t_{TRANSITION}$	R_L = 100 Ω, C_L = 35 pF		140					
		V_S = 10 V, See FIGURE 9			170			240	
Break before Make time delay	t_{BBM}	R_L = 100 Ω, C_L 35 pF,		50					
		$V_{S1} = V_{S2}$ = 10 V, See FIGURE 10				19			
	t_{ON} (EN)	R_L = 100 Ω, C_L = 35 pF		100					
		V_S = 10 V, See FIGURE 11			120			165	
	t_{OFF} (EN)	R_L = 100 Ω, C_L = 35 pF		100					
		V_S = 10 V, See FIGURE 11			120			170	
Charge injection		V_S = 0 V, R_S = 0 Ω, C_L = 1 nF; See FIGURE 12		-50					pC
Off isolation		R_L = 50 Ω, C_L 5 pF, f = 1 MHz, See FIGURE 13		-70					dB
Channel to channel crosstalk		R_L = 50 Ω, C_L 5 pF, f = 1 MHz, See FIGURE 14		-70					dB
Total harmonic distortion, THD + N		R_L = 110 Ω, 15 V p-p, f = 20 Hz to 20 kHz, See FIGURE 16		0.025					%
-3 dB Bandwidth		R_L = 50 Ω, C_L 5 pF, See FIGURE 15		115					MHz
Insertion loss		R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, See FIGURE 15		0.24					dB
C_S (Off)		f = 1 MHz		14					pF
C_D (Off)				40					
C_D, C_S (ON)				90					
Power requirements (V_{DD} = +16.5 V, V_{SS} = -16.5 V)									
	I_{DD}	Digital inputs = 0 V or V_{DD}		0.002				1	µA
		Digital inputs = 5 V		220				420	
	I_{SS}	Digital inputs = 0 V, 5 V or V_{DD}		0.002				1	
	V_{DD}/V_{SS}				±4.5			±16.5	V

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test conditions **12 V Single Supply** 4/	Limits						Unit
			+25°C			-55°C to +125°C			
			Min	Typ	Max	Min	Typ	Max	
Analog switch									
Analog signal range						0		V_{DD}	V
On Resistance	R_{ON}	V_S = 0 V to10 V, I_S = -10 mA; See FIGURE 6		6					Ω
		V_{DD} = 10.8 V, V_{SS} = 0 V			8			11.2	
On resistance match between channels	Δ R_{ON}	V_S = 0 V to 10 V, I_S = -10 mA		0.2					Ω
					0.82			1.1	
On resistance Flatness	$R_{FLAT(ON)}$	V_S = 0 V to10 V, I_S = -10 mA		1.5					Ω
					2.5			2.8	
Leakage current I_S (Off) (V_{DD} = 13.2 V)									
Source off leakage	I_S (Off)	V_S = 1V/10 V, V_D = 10 V/1 V; See FIGURE 7		±0.04					nA
					±0.2			±5	
Drain off leakage	I_D (Off)	V_S = 1V/10 V, V_D = 10 V/1 V; See FIGURE 7		±0.04					
					±0.45			±37	
Channel On leakage	I_D, $I_{S\ (ON)}$	V_S = V_D = 1 V or 10 V, See FIGURE 8		±0.06					
					±0.44			±32	
Digital inputs									
Input high voltage	V_{IH}					2.0			V
Input low voltage	V_{IL}							0.8	
Input current	I_{NL} or I_{NH}	V_{IN} = V_{GND} or V_{DD}		±0.005					µA
								±0.1	
Digital input capacitance	C_{IN}			5					pF

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test conditions **12 V Single Supply - Continued** 4/	Limits						Unit
			+25°C			-55°C to +125°C			
			Min	Typ	Max	Min	Typ	Max	
Dynamic characteristics 3/									
Transition time	$t_{TRANSITION}$	R_L = 100 Ω, C_L = 35 pF,		200					ns
		V_S = 8 V, See FIGURE 9			260			380	
Break before Make time delay	t_{BBM}	R_L = 100 Ω, C_L 35 pF,		90					
		V_{S1} = V_{S2} = 8 V, See FIGURE 10				40			
	t_{ON} (EN)	R_L = 100 Ω, C_L = 35 pF,		160					
		V_S = 8 V, See FIGURE 11			210			285	
	t_{OFF} (EN)	R_L = 100 Ω, C_L = 35 pF,		115					
		V_S = 8 V, See FIGURE 11			145			200	
Charge injection		V_S = 6 V, R_S = 0 Ω, C_L = 1 nF; See FIGURE 12		-12					pC
Off isolation		R_L = 50 Ω, C_L 5 pF, f = 1 MHz, See FIGURE 13		-70					dB
Channel to channel crosstalk		R_L = 50 Ω, C_L 5 pF, f = 1 MHz, See FIGURE 14		-70					dB
-3 dB Bandwidth		R_L = 50 Ω, C_L 5 pF, See FIGURE 15		72					MHz
Insertion loss		R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, See FIGURE 15		0.5					dB
C_S (Off)		f = 1 MHz		25					pF
C_D (Off)				80					
C_D, C_S (ON)				120					
Power requirements (V_{DD} = 13.2 V)									
	I_{DD}	Digital inputs = 0 V or V_{DD}		0.002				1	µA
		Digital inputs = 5 V		220				420	
	V_{DD}/V_{SS}	V_{SS} = 0 V, GND = 0 V				5		16.5	V

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test conditions **5 V Dual Supply** 5/	Limits						Unit
			+25°C			-55°C to +125°C			
			Min	Typ	Max	Min	Typ	Max	
Analog switch									
Analog signal range						V_{SS}		V_{DD}	V
On Resistance	R_{ON}	V_S = ±4.5 V, I_S = -10 mA; See FIGURE 6		7					Ω
		V_{DD} = +4.5 V, V_{SS} = -4.5 V			9			12	
On resistance match between channels	Δ R_{ON}	V_S = ±4.5 V, I_S = -10 mA		0.3					Ω
					0.78			1.1	
On resistance Flatness	$R_{FLAT(ON)}$	V_S = ±4.5 V, I_S = -10 mA		1.5					Ω
					2.5			3	
Leakage current I_S (Off) (V_{DD} = +5.5 V, V_{SS} = -5.5 V)									
Source off leakage	I_S (Off)	V_S = ±4.5 V, V_D = ∓4.5 V; See FIGURE 7		±0.02					nA
					±0.2			±5	
Drain off leakage	I_D (Off)	V_S = ±4.5 V, V_D = ∓4.5 V; See FIGURE 7		±0.02					
					±0.45			±20	
Channel On leakage	I_D, $I_{S (ON)}$	V_S = V_D = ±4.5 V, See FIGURE 8		±0.04					
					±0.3			±22	
Digital inputs									
Input high voltage	V_{IH}					2.0			V
Input low voltage	V_{IL}							0.8	
Input current	I_{NL} or I_{NH}	V_{IN} = V_{GND} or V_{DD}		±0.005					µA
								±0.1	
Digital input capacitance	C_{IN}			5					pF

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test conditions **5 V Dual Supply - Continued** 5/	Limits						Unit
			+25°C			-55°C to +125°C			
			Min	Typ	Max	Min	Typ	Max	
Dynamic characteristics 3/									
Transition time	$t_{TRANSITION}$	R_L = 100 Ω, C_L = 35 pF, V_S = 5 V, See FIGURE 9		330					ns
					440			550	
Break before Make time delay	t_{BBM}	R_L = 100 Ω, C_L 35 pF, V_{S1} = V_{S2} = 5 V, See FIGURE 10		100					
						45			
	t_{ON} (EN)	R_L = 100 Ω, C_L = 35 pF, V_S = 5 V,See FIGURE 11		245					
					330			440	
	t_{OFF} (EN)	R_L = 100 Ω, C_L = 35 pF, V_S = 5 V,See FIGURE 11		215					
					285			370	
Charge injection		V_S = 0 V, R_S = 0 Ω, C_L = 1 nF; See FIGURE 12		-10					pC
Off isolation		R_L = 50 Ω, C_L 5 pF, f = 1 MHz, See FIGURE 13		-70					dB
Channel to channel crosstalk		R_L = 50 Ω, C_L 5 pF, f = 1 MHz, See FIGURE 14		-70					dB
Total harmonic distortion, THD + N		R_L = 110 Ω, 5 V p-p, f = 20 Hz to 20 kHz, See FIGURE 16		0.06					%
-3 dB Bandwidth		R_L = 50 Ω, C_L 5 pF, See FIGURE 15		80					MHz
Insertion loss		R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, See FIGURE 15		0.5					dB
C_S (Off)		f = 1 MHz		20					pF
C_D (Off)				65					
C_D, C_S (ON)				120					
Power requirements (V_{DD} = +5.5 V, V_{SS} = -5.5 V)									
	I_{DD}	Digital inputs = 0 V or V_{DD}		0.001				1	µA
	I_{SS}	Digital inputs = 0 V, 5 V or V_{DD}		0.001				1	
	V_{DD}/V_{SS}				±4.5			±16.5	V

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

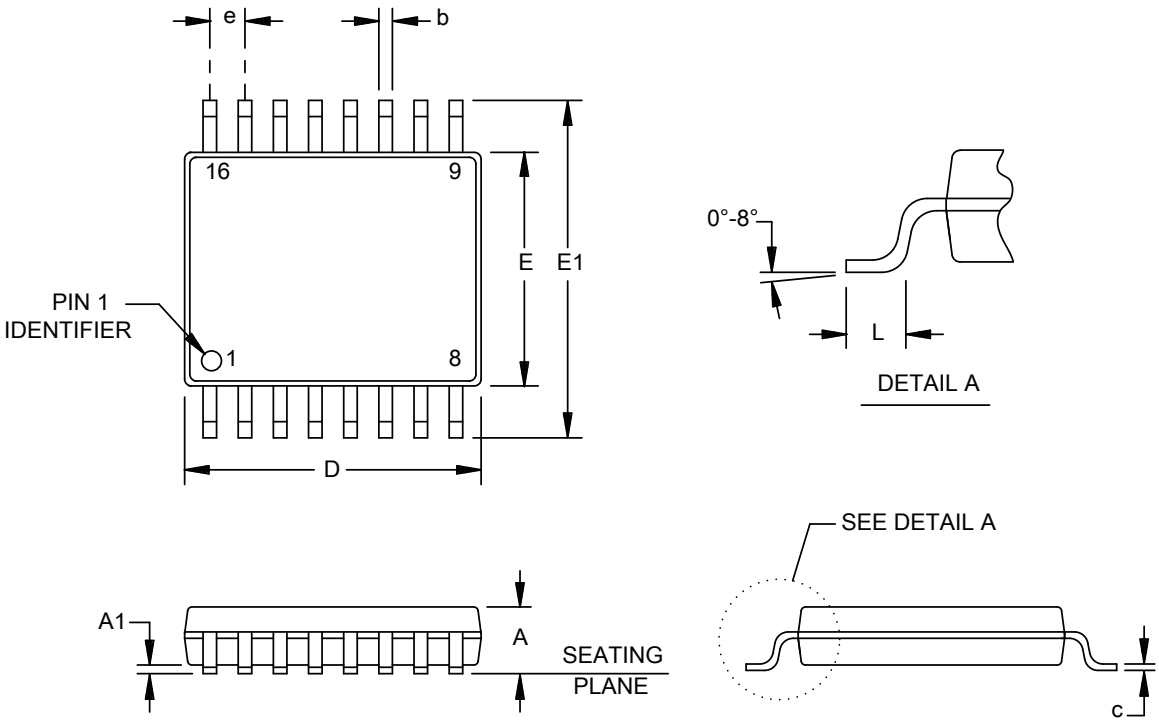
2/ V_{DD} = +15 V ±10%, V_{SS} = -15 V ±10%, GND = 0 V, unless otherwise noted.

3/ Guaranteed by design, not subject to production test.

4/ V_{DD} = +12 V ±10%, V_{SS} = 0 V, GND = 0 V, unless otherwise noted.

5/ V_{DD} = +5 V ±10%, V_{SS} = -5 V ±10%, GND = 0 V, unless otherwise noted

Case X



Dimensions					
Symbol	Millimeters		Symbol	Millimeters	
	Min	Max		Min	Max
A		1.20	E	4.30	4.50
A1	0.05	0.15	E1	6.40 BSC	
b	0.19	0.30	e	0.65 BSC	
c	0.09	0.20	L	0.45	0.75
D	4.90	5.10			

NOTES:
1. All linear dimensions are in millimeters.
2. Falls within JEDEC MO-15-AB3.

FIGURE 1. Case outline.

Case outline X			
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	A0	16	A1
2	EN	15	GND
3	V_{SS}	14	V_{DD}
4	S1A	13	S1B
5	S2A	12	S2B
6	S3A	11	S3B
7	S4A	10	S4B
8	DA	9	DB

FIGURE 2. Terminal connections.

Case outline X		
Terminal		Description
No	Mnemonic	
1	A0	Logic control input
2	EN	Active high digital input. When low, the device is disabled and all switches are off. When high, Ax logic inputs determine on switches
3	V_{SS}	Most negative power supply potential. In single supply applications, it can be connected to ground
4	S1A	Source terminal 1A. Can be an input or an output.
5	S2A	Source terminal 2A. Can be an input or an output.
6	S3A	Source terminal 3A. Can be an input or an output.
7	S4A	Source terminal 4A. Can be an input or an output.
8	DA	Drain terminal A. Can be an input or an output.
9	DB	Drain terminal B. Can be an input or an output.
10	S4B	Source terminal 4B. Can be an input or an output.
11	S3B	Source terminal 3B. Can be an input or an output.
12	S2B	Source terminal 2B. Can be an input or an output.
13	S1B	Source terminal 1B. Can be an input or an output.
14	V_{DD}	Most positive power supply potential.
15	GND	Ground (0 V) reference.
16	A1	Logic control input

FIGURE 3. Terminal function.

Device type 02			
A1	A0	EN	On Switch Pair
X	X	0	None
0	0	1	1
0	1	1	2
1	0	1	3
1	1	1	4

FIGURE 4. Truth table

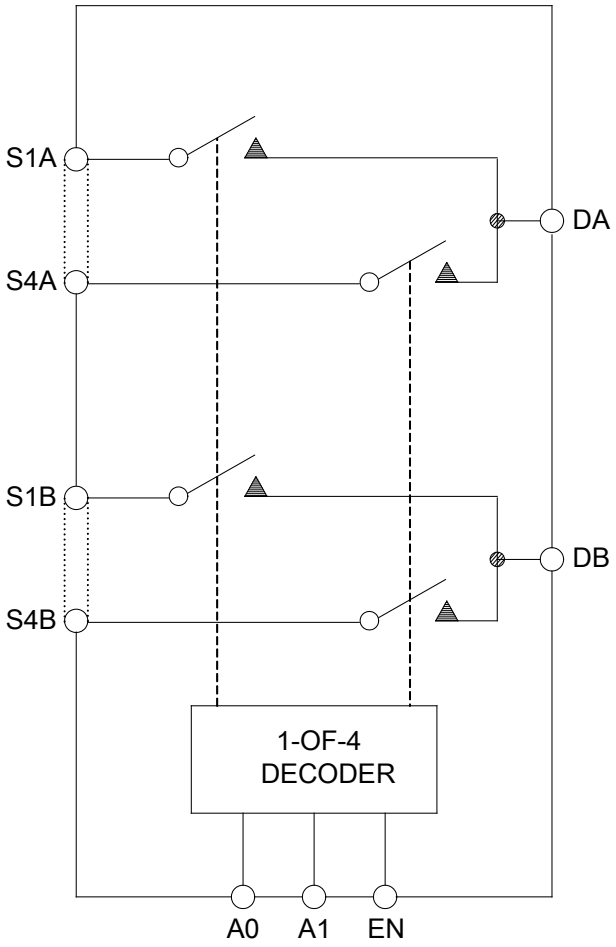


FIGURE 5. Functional block diagram.

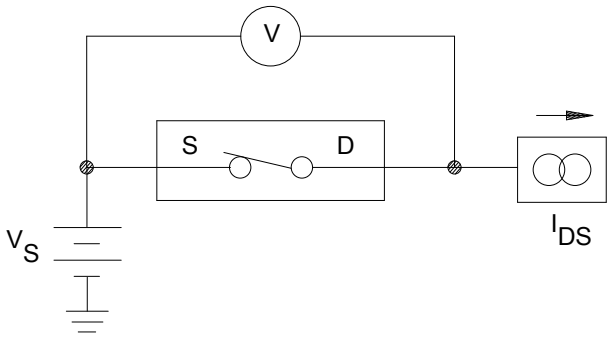


FIGURE 6. On resistance.

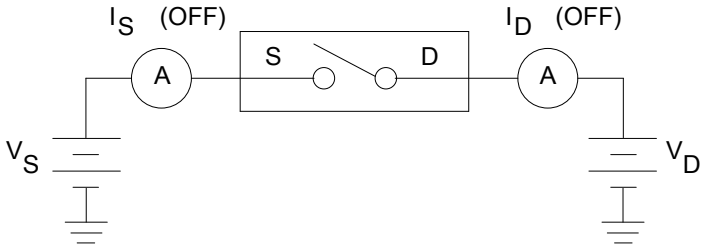


FIGURE 7. Off leakage.

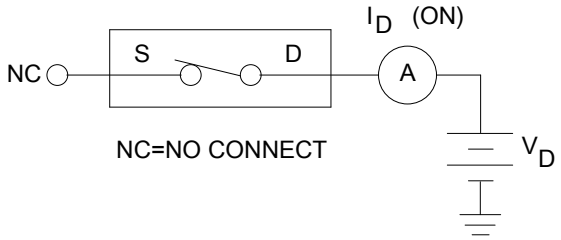


FIGURE 8. On leakage.

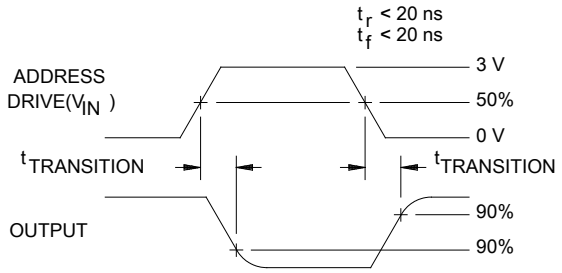


FIGURE 9. Address to output switching times, $t_{TRANSITION}$.

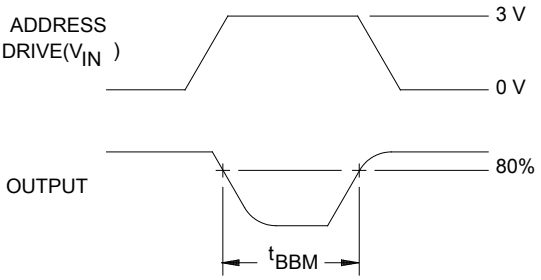


FIGURE 10. Break before make time delay, t_{BBM}.

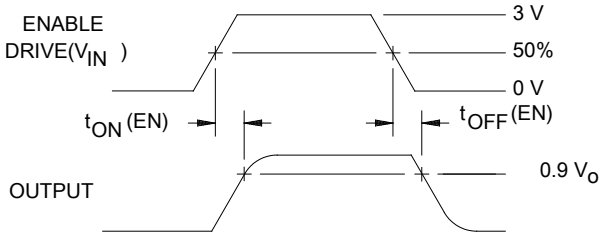


FIGURE 11. Enable delay, t_{ON} (EN), t_{OFF} (EN).

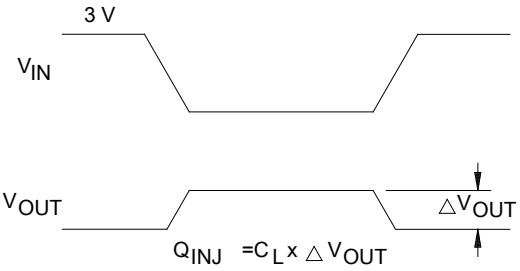


FIGURE 12. Charge Injection.

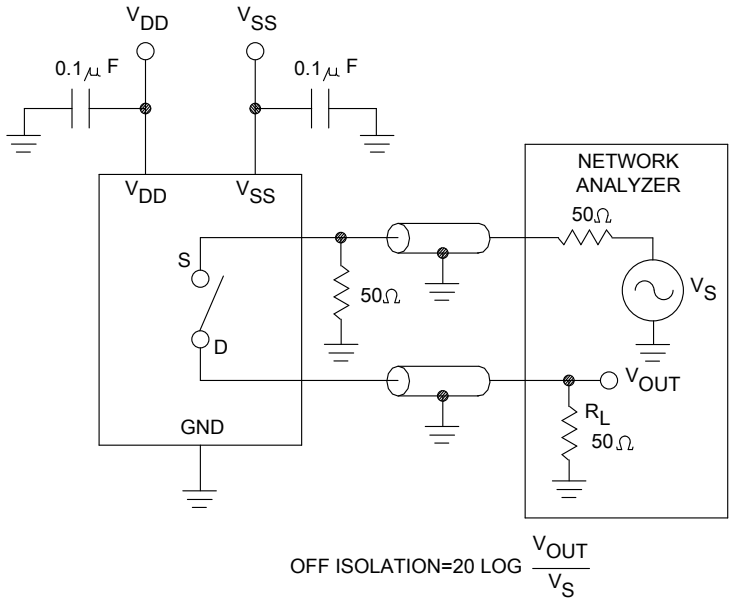


FIGURE 13. Off isolation.

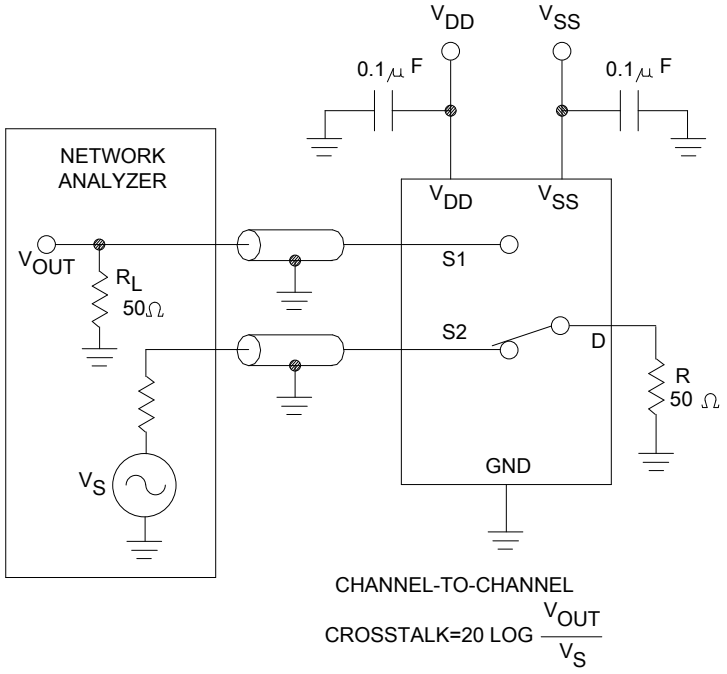
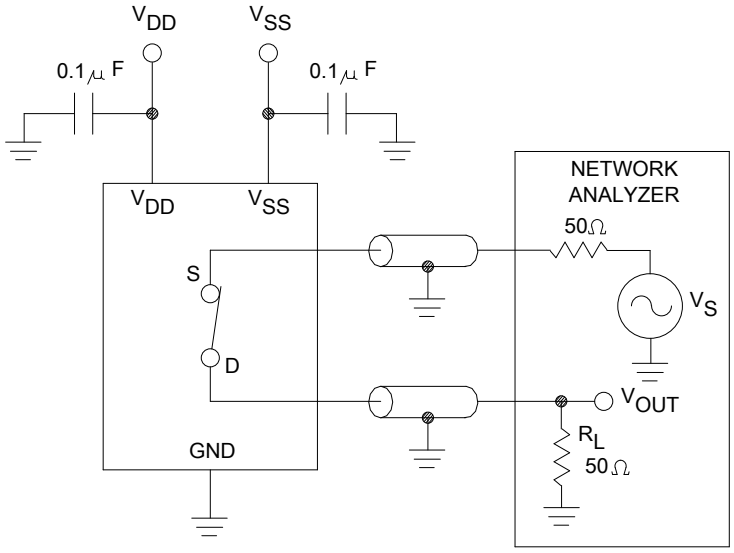


FIGURE 14. Channel to Channel crosstalk.



$$\text{INSERTION LOSS} = 20 \log \frac{V_{OUT} \text{ WITH SWITCH}}{V_{OUT} \text{ WITHOUT SWITCH}}$$

FIGURE 15. Insertion loss.

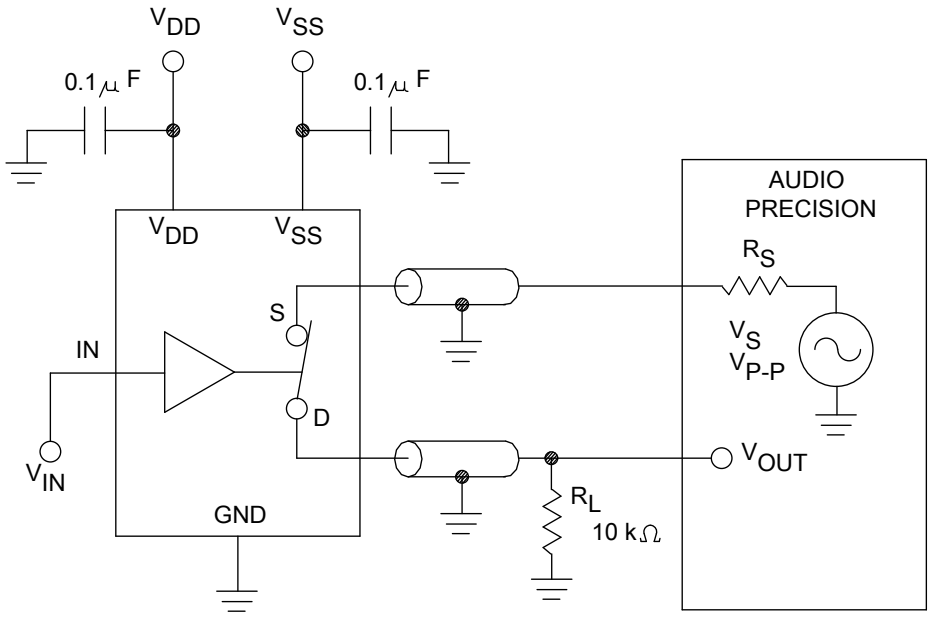


FIGURE 16. THD + Noise.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.landandmaritime.dla.mil/Programs/Smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Vendor part number
V62/12652-01XB	24355	ADG1409SRU-EP-RL7

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.
2/ Not available from an approved source of supply.

CAGE code	Source of supply
24355	Analog Devices 1 Technology Way P.O. Box 9106 Norwood, MA 02062-9106